



# The Fusion Of Hardware Design And Verification

**Allen Kent, James G. Williams**



## **The Fusion Of Hardware Design And Verification:**

**The Fusion of Hardware Design and Verification** George J. Milne, 1988 The Fusion of Hardware Design and Verification George J. Milne, Fédération internationale pour le traitement de l'information. Working Group 10.2, International Federation for Information Processing. Working Group 10.2, 1988

**Designing Correct Circuits** Geraint Jones, Mary Sheeran, 2013-12-14 These proceedings contain the papers presented at a workshop on Designing Correct Circuits jointly organised by the Universities of Oxford and Glasgow and held in Oxford on 26-28 September 1990. There is a growing interest in the application to hardware design of the techniques of software engineering. As the complexity of hardware systems grows and as the cost both in money and time of making design errors becomes more apparent, so there is an eagerness to build on the success of mathematical techniques in program development. The harsher constraints on hardware designers mean both that there is a greater need for good abstractions and rigorous assurances of the trustworthiness of designs and also that there is greater reason to expect that these benefits can be realised. The papers presented at this workshop consider the application of mathematics to hardware design at several different levels of abstraction. At the lowest level of this spectrum, Zhou and Hoare show how to describe and reason about synchronous switching circuits using UNILY, a formalism that was developed for reasoning about parallel programs. Aagaard and Leeser use standard mathematical techniques to prove correct their implementation of an algorithm for Boolean simplification. The circuits generated by their formal synthesis system are thus correct by construction. Thuau and Pilaud show how the declarative language LUSTRE, which was designed for programming real-time systems, can be used to specify synchronous circuits.

**Correct Hardware Design and Verification Methods**, 1993 **Encyclopedia of Microcomputers** Allen Kent, James G. Williams, 1997-05-21 Visual Fidelity Designing Multimedia Interfaces for Active Learning to Xerox Corporation *Formal Methods in Circuit Design* Victoria Stavridou, 1993-07-22 Graduate level account of hardware verification and algebraic specification

**Formal Verification of Hardware Design** Michael Yoeli, 1990 **Correct Hardware Design Methodologies** Paolo Prinetto, Paolo Camurati, 1992 The increasing interest in formal verification of hardware is witnessed by academic and industrial research efforts, multinational research projects and conferences. These proceedings contain the papers presented at the Workshop held in Turin, Italy, from 12-14 June 1991. Papers focus on the practical impact of formal techniques in VLSI design and verification semantics for hardware description languages, proof environments and methodologies. Preliminary results of the ESPRIT Basic Research Action 3216 CHARME are discussed. Finite State Machines and their verification semantics for hardware description languages, proof environments and methodologies, as well as examples of verified circuits and Design for Verifiability, are also presented.

Computer Aided Verification Pierre Wolper, 1995-06-21 This volume constitutes the proceedings of the 7th International Conference on Computer Aided Verification (CAV 95) held in Liège, Belgium, in July 1995. The book contains the 31 refereed full research papers selected for presentation at CAV 95, as well as abstracts or full papers.

of the three invited presentations Originally oriented towards finite state concurrent systems CAV now covers all styles of verification approaches and a variety of application areas The papers included range from theoretical issues to concrete applications with a certain emphasis on verification tools and the algorithms and techniques needed for their implementations Beyond finite state systems real time systems and hybrid systems are an important part of the conference

**Theorem Provers in Circuit Design** Victoria Stavridou, Tom F. Melham, Raymond T. Boute, 1992 The papers in this volume address the role of mechanized theorem proving technology in the design of digital systems The primary focus is on the practical application of theorem provers to digital design rather than on theoretical foundations The diverse contributions include invited papers by the leading researchers Gordon and Hunt as well as technical contributions by many other prominent researchers in the field of machine assisted hardware verification This side of the Proceedings reflects current research activity and the section containing tutorial papers on several influential theorem provers serves as an introduction to this exciting field

A Framework for the Specification, Design, and Verification of Pipelines with Structural Hazards

Mark Aagaard, 1995 Design Methodologies for VLSI and Computer Architecture Doug A. Edwards, 1989 *Computer Hardware Description Languages and Their Applications* John A. Darringer, F. J. Rammig, 1990 Languages for precisely describing the behavior of computers have been studied since the conception of the computer itself As the computer industry has grown so has the need to exchange information about computers Computer Hardware Description Languages CHDL are required to provide specifications and detailed implementation for a growing menu of sophisticated design automation tools including synthesis verification simulation analysis optimization placement wiring and testing communicate requirements and capabilities between suppliers and users of computer components and subsystems facilitate the transfer of new methods and results within the university and industrial research community As reflected in this book there is an increased emphasis on applications and resulting requirements that are placed on CHDLs In the field of synthesis a major application area there is today a focus on high level synthesis and synthesis under design constraints In the area of design correctness research has shifted away from simulation to formal verification techniques such as temporal logic

**Mechanized Reasoning and**

**Hardware Design** Charles Antony Richard Hoare, Michael J. C. Gordon, 1992 The result of a Royal Society Discussion this book explores the ways in which mechanized reasoning tools can be used to implement good design It examines the interplay between logic and tools exploring theoretical possibilities costs and practical benefits

**Computer Hardware**

**Description Languages and Their Applications** Dominique Borrione, Ron Waxman, 1991 The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling including simulation verification by correctness proofs synthesis and test The strong relationship between the topics of CHDL 91 and the work around the use and re standardization of the VHDL language is also explored The quality of this proceedings and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled

**Designing Correct Circuits** Jørgen Staunstrup, Robin Sharp, 1992 The papers compiled in this volume cover a wide range of topics within the general area of provably correct design including proofs of fundamental results post hoc formal verification of designs and design techniques where correctness is ensured by construction The papers are unique in that they demonstrate the use of design techniques for designing real chips The book should thus not be missed by students and researchers interested in the deployment of formally based techniques on real problems within a great diversity of application areas Application areas treated within the volume range from packet routers arbiters multiprocessors serial parallel converters and CPUs to arithmetic units and counters A significant group of the papers is concerned with the special requirements of asynchronous and delay insensitive design

**Transformational Approaches to Systolic Design** G. M. Megson, 1994 Computer Systems Organization Processor Architectures

Hardware Design Verification William K. C. Lam, 2005 The Practical Start to Finish Guide to Modern Digital Design Verification As digital logic designs grow larger and more complex functional verification has become the number one bottleneck in the design process Reducing verification time is crucial to project success yet many practicing engineers have had little formal training in verification and little exposure to the newest solutions Hardware Design Verificationsystematically presents today s most valuable simulation based and formal verification techniques helping test and design engineers choose the best approach for each project quickly gain confidence in their designs and move into fabrication far more rapidly College students will find that coverage of verification principles and common industry practices will help them prepare for jobs as future verification engineers Author William K Lam one of the world s leading experts in design verification is a recent winner of the Chairman s Award for Innovation Sun Microsystems most prestigious technical achievement award Drawing on his wide ranging experience he introduces the foundational principles of verification presents traditional techniques that have survived the test of time and introduces emerging techniques for today s most challenging designs Throughout Lam emphasizes practical examples rather than mathematical proofs wherever advanced math is essential he explains it clearly and accessibly Coverage includes Simulation based versus formal verification advantages disadvantages and tradeoffs Coding for verification functional and timing correctness syntactical and structure checks simulation performance and more Simulator architectures and operations including event driven cycle based hybrid and hardware based simulators Testbench organization design and tools creating a fast efficient test environment Test scenarios and assertion planning test cases test generators commercial and Verilog assertions and more Ensuring complete coverage including code parameters functions items and cross coverage The verification cycle failure capture scope reduction bug tracking simulation data dumping isolation of underlying causes revision control regression release mechanisms and tape out criteria An accessible introduction to the mathematics and algorithms of formal verification from Boolean functions to state machine equivalence and graph algorithms Decision diagrams equivalence checking and symbolic simulation Model checking and symbolic computation Simply put Hardware

Design Verification will help you improve and accelerate your entire verification process from planning through tape out so you can get to market faster with higher quality designs      *Comp Euro* ,1991      *Mathematical Foundations of Computer Science* ,1992

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